14. (Amended) The method in accordance with claim 13 further comprising a step of:

d. cutting the semiconductor wafer vertically along a horizontal saw-line extending across the hole such that a portion of the semiconductor wafer containing the IC includes a peripheral edge formed along the saw-line upon which a portion of the first conductive material placed in the hole remains attached.

15. (Amended) The method in accordance with claim 14 further comprising a step of:

e. forming a bond pad on the lower surface of the semiconductor wafer conductively linked to the conductive material placed in the hole.

16. (Amended) The method in accordance with claim 14 further comprising a step of:

e. providing second conductive material extending horizontally from the first conductive material along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing the IC.

17. (Amended) The method in accordance with claim 14 wherein step c comprises a step of:

e. providing second conductive material extending horizontally on the upper surface of the semiconductor wafer and on the IC from the first conductive material to the first circuit node.

A1 concluded

18. (Amended) The method in accordance with claim 17 further comprising a step of:

~~f.~~ providing third conductive material extending horizontally from the first conductive material along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing ~~the IC.~~

Add new claims as follows:

33. (New) A method for fabricating an interconnect system for providing signal paths between a plurality of circuit nodes on horizontal upper surfaces of a plurality of integrated circuit IC dice formed within and on a semiconductor wafer and horizontal lower surfaces of the IC dice, the method comprising the steps of:

A2

a. forming a plurality of holes extending vertically through the semiconductor wafer in areas of the semiconductor wafer between the IC dice,

b. placing first conductive material in the holes formed in the semiconductor wafer, and

c. placing second conductive material on the upper surfaces of said IC dice, the second conductive material forming signal paths extending horizontally between the circuit nodes and the first conductive material in the holes placed in the holes.

34. (New) The method in accordance with claim 33 further comprising the step of:

d. cutting on the wafer in the areas between the dice so as to singulate the IC dice and so that portions of the first conductive material remain on the IC dice after they are singulated to provide conductive paths between the second conductive material on the upper surfaces of the IC dice and the lower surfaces of the IC dice.

35. (New) The method in accordance with claim 34 further comprising the step of:

e. prior to cutting the wafer at step d, forming conductive pads on the lower surfaces of the IC dice that are conductively linked to the first conductive material placed in the holes.

In the Abstract:

Amend the abstract to read as follows:

A method for forming an integrated circuit (IC) interconnect system is described in which vertical holes are created in streets separating individual integrated circuit IC dice formed on a semiconductor wafer. The holes span saw-lines along which the wafer is to be later cut to separate the IC die from one another to form individual IC chips. The holes are then filled with conductive material. After the wafer is cut along the saw-lines, portions of the conductive material on opposing sides of the saw-lines remain on peripheral edges of the IC chip to form signal paths between the upper and lower surfaces of the IC chips.